CLAIMS

What is claimed is:

1. A method of programming memory cells of a memory device, the method comprising selectively depositing insulating layers over parts of a first portion of the memory cells while not depositing insulating layers over parts of a second portion of the memory cells, to thereby program the memory device.

2. The method as set forth in claim 1, wherein the parts are electrodes.

3. The method as set forth in claim 1, wherein the parts are channels.

4. The method as set forth in claim 1, wherein the parts are gate electrodes.

5. The method as set forth in claim 4, wherein:
the memory cells are transistors;
word lines extend over the gate electrodes;
gate electrodes of the first portion of the memory cells are not connected to the word lines; and
gate electrodes of the second portion of the memory cells are connected to the word lines.

6. A method of programming a memory device having a plurality of memory cells positioned to be coupled to corresponding word lines, the method comprising coupling only predetermined ones of the plurality of memory cells to their corresponding word lines and leaving other memory cells of the plurality of memory cells relatively decoupled from their corresponding word lines.

7. The method as set forth in claim 6, wherein:
the predetermined ones of the plurality of memory cells are not disabled; and

the other memory cells of the plurality of memory cells are disabled.

8. The method as set forth in claim 6, wherein insulating layers are disposed between the relatively decoupled memory cells and their corresponding word lines, but are not disposed between the coupled memory cells and their corresponding word lines.

9. The method as set forth in claim 8, wherein:

each memory cell comprises a transistor having two source/drain regions and a gate; and

the insulating layers are disposed between gates of the relatively decoupled memory cells and their corresponding word lines.

10. The method as set forth in claim 6, wherein substantially all of the memory cells of the memory device have substantially the same threshold voltages.

11. The method as set forth in claim 6, wherein substantially none of the memory cells of the memory device are ion-implantation coded.

12. A memory device fabricated according to the method of claim 6.

13. A method of programming a memory device comprising disabling predetermined memory cells of the memory device by electrically insulating the predetermined memory cells from word lines of the memory device to which the predetermined memory cells would otherwise be electrically coupled but for the disabling, whereby non-disabled memory cells of the memory device are not insulated from, or are insulated to a lesser extent from, corresponding word lines of the memory device.

14. The method as set forth in claim 13, wherein a first portion of memory cells corresponding to a word line are disabled and a second portion of memory cells corresponding to the same word line are not disabled.

15. The method as set forth in claim 13, wherein insulating layers are disposed between channels of the disabled memory cells and their corresponding word lines, but are not disposed between channels of the non-disabled memory cells and their corresponding word lines.

16. The method as set forth in claim 13, wherein:

each memory cell comprises a transistor having two source/drain regions and a gate;

insulating layers are disposed between gates of the disabled memory cells and their corresponding word lines; and

insulating layers are not disposed between gates of the non-disabled memory cells and their corresponding word lines.

17. The method as set forth in claim 13, wherein the method further comprises:

providing a substrate having a first surface;

creating a dielectric layer on the first surface of the substrate;

forming a plurality of substantially parallel strip-stacked layers on the dielectric layer, each strip-stacked layer comprising a disposable layer formed on a gate electrode layer, the gate electrode layer of each strip-stacked layer being disposed on the dielectric layer;

forming a plurality of source/drain regions in the substrate, each source/drain region being adjacent to the first surface of the substrate, wherein each strip-stacked layer is disposed substantially between a pair of adjacent source/drain regions;

forming a plurality of first spacers on the dielectric layer, each of the first spacers being disposed between two adjacent strip-stacked layers;

patterning the strip-stacked layers to form a plurality of gate electrodes disposed on the dielectric layer and a plurality of disposable pillars disposed on the gate electrodes, wherein portions of the strip-stacked layers are removed thereby creating a plurality of apertures;

forming a plurality of second spacers within the apertures;

removing the plurality of the disposable pillars to form a plurality of openings that expose the plurality of gate electrodes;

forming a patterned mask to cover the gate electrodes corresponding to active code positions of the memory device in accordance with the code; and

wherein the disabling of predetermined memory cells further comprises depositing insulating layers on the gate electrodes corresponding to inactive code positions of the memory device in accordance with the code, removing the patterned mask, and forming a plurality of word lines interconnecting the gate electrodes corresponding to the active code positions, each word line being disposed substantially perpendicularly to the source/drain regions, the gate electrodes corresponding to the inactive code positions being electrically isolated from the word lines.

18. The method as set forth in claim 17, wherein:

portions of the first spacers are removed during the step of patterning; and

the forming of a plurality of second spacers comprises forming a plurality of second spacers in place of at least the portions of the first spacers that have been removed.

19. The method as set forth in claim 18, wherein:

the forming of a plurality of substantially parallel strip-stacked layers comprises forming a plurality of polysilicon gate electrode layers and a plurality of silicon nitride disposable layers;

the depositing of insulating layers comprises spin-on coating silicon dioxide insulating layers;

the forming of a patterned mask comprises forming a patterned photoresist mask;

the forming of a plurality of first spacers comprises forming a plurality of first silicon dioxide spacers; and

the forming of a plurality of second spacers comprises forming a plurality of second silicon dioxide spacers.

20. A memory device fabricated according to the method of claim 13.

21. A memory device fabricated according to the method of claim 17.

22. A semiconductor memory device coded by selective deposition of insulating layers on gate electrodes of transistor memory cells of the device.

23. A mask read-only memory (ROM), comprising:

a substrate;

a plurality of buried drains disposed in the substrate;

a dielectric layer disposed on the substrate, the dielectric layer having a plurality of openings exposing code positions of the mask ROM;

a plurality of gates disposed in the openings;

a plurality of insulating layers disposed on selected ones of the plurality of gates, which are located at non-real code positions of the mask ROM; and

a plurality of word lines disposed on the openings and the dielectric layer, wherein the word lines are substantially perpendicular to the buried drains.

24. A memory device coded by the existence of insulating layers over parts of a first portion of the memory cells and an absence of such insulating layers over corresponding parts of a second portion of the memory cells.

25. The memory device as set forth in claim 24, wherein the parts are electrodes.

26. The memory device as set forth in claim 24, wherein the parts are channels.

27. The memory device as set forth in claim 24, wherein the parts are gate electrodes.

28. The memory device as set forth in claim 27, wherein:

the memory cells are transistors;

word lines extend over the gate electrodes;

gate electrodes of the first portion of the memory cells are not connected to the word lines; and

gate electrodes of the second portion of the memory cells are connected to the word lines.

29. The memory device as set forth in claim 27, and further comprising:

a semiconductor substrate of first type majority carriers, the substrate comprising a first surface and a plurality of substantially parallel elongated buried source/drain regions adjacent to the first surface, the source/drain regions having second type majority carriers;

a dielectric gate layer disposed on the first surface of the substrate; and

a plurality of electrically conducting word lines disposed over the gate electrodes of the first and second portions of the memory cells;

wherein the gate electrodes of the first and second portions of the memory cells are disposed in rows and columns on the dielectric gate layer, each row being disposed substantially between two adjacent source/drain regions and the columns being substantially perpendicular to the rows, each gate electrode being disposed on a different code position and comprising a first end surface adjacent to the dielectric gate layer and a second end surface opposite the first end surface, the insulating layers being disposed on the second end surfaces of the gate electrodes of the first portion of the memory cells, the gate electrodes of the first portion of the memory cells corresponding to inactive code positions of the coded memory device and the gate electrodes of the second portion of the memory cells corresponding to active code positions of the coded memory device, the word lines being connected to gate electrodes of the second portion of the memory cells and being electrically insulated by the insulating layers from the gate electrodes of the first portion of the memory cells.

30. The memory device as set forth in claim 29, wherein:

the gate electrodes comprise polysilicon;

spacers comprising silicon dioxide are disposed between the gate electrodes; and

an encapsulating material covers the word lines, the gate electrodes, and the spacers.